Investigation of Hybrid Multilevel Inverter Performance via FFT Analysis Implemented in Simulation

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Abstract: *This paper presents a comparative study of various hybrid multilevel inverter (HMLI) configurations with respect to their output voltage levels and overall performance. The focus is on harmonic elimination in HMLIs to reduce the total harmonic distortion (THD) of the voltage applied to the load, thereby improving power quality [1,2]. Different HMLI topologies are analyzed and compared, emphasizing their effectiveness in minimizing harmonics. By dividing the switching process into high- and low-frequency components, the proposed approach aims to enhance converter efficiency while simultaneously reducing size and cost [3]. Furthermore, this study introduces the performance analysis of a novel hybrid multilevel inverter topology, referred to as SHMLI, employing various pulse width modulation (PWM) strategies. The PWM techniques investigated include multicarrier phase disposition (PD) and phase shift modulation methods, which have been demonstrated to improve switching performance and harmonic profile [4,5]. All simulations and analyses are conducted using MATLAB-SIMULINK to validate the theoretical findings.*

Keywords: *Hybrid Multilevel Inverter (HMLI), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM), Phase Disposition (PD), Symmetrical Hybrid Multilevel Inverter (SHMLI)*

I. INTRODUCTION

Multilevel inverters have gained significant attention in recent years due to their ability to synthesize high-quality voltage waveforms with reduced harmonic distortion, making them suitable for high-power and medium-voltage applications [1]. Unlike traditional two-level inverters, multilevel inverters generate output voltages with multiple steps, which results in a staircase waveform that more closely approximates a sinusoidal waveform, thereby improving power quality and reducing electromagnetic interference [2].

Among the various multilevel inverter topologies, hybrid multilevel inverters (HMLIs) have emerged as a promising solution combining the advantages of both diode-clamped and cascaded H-bridge configurations [3]. HMLIs offer enhanced performance by efficiently managing switching losses through the division of the switching process into high-frequency and low-frequency components, which leads to improved converter efficiency and reduced overall system size and cost [3].

Furthermore, the application of advanced pulse width modulation (PWM) strategies such as multicarrier phase disposition and phase shift modulation has been shown to significantly improve the harmonic profile and switching performance of HMLIs [4,5]. These modulation techniques enable better control over voltage levels and switching sequences, facilitating harmonic elimination and contributing to the reduction of total harmonic distortion (THD) in the output voltage.
MLIs generate a staircase output voltage waveform by the proper combinations of multiple input DC sources and power semiconductor devices [15]. Therefore, MLIs presents a better operation compared to two-level converters listed as follows [16,18].

1. Easy extension because of modular structure.
2. Better harmonic specification and significantly reduces the filter size due to generation a waveform as close to a sinusoidal waveform as possible.

3. Reduction of the voltage stress (dv/dt); which can alleviate the problems related to Electromagnetic Interference (EMI).
4. Lower switching losses as a result of lower switching frequency and the lower voltage stress on the devices.

This paper focuses on analyzing different HMLI configurations and evaluating their performance in terms of output voltage levels, harmonic distortion, and efficiency. The study also investigates the performance of a novel hybrid multilevel inverter topology using different PWM strategies, with simulation results obtained via MATLAB-SIMULINK to validate the proposed approaches. [19,20]

II. SINGLE-PHASE SYMMETRICAL HYBRID MULTILEVEL INVERTER (SHMLI)

Single-phase symmetrical hybrid multilevel inverters (SHMLIs) utilize equal DC voltage sources to generate multiple voltage levels. As explained by Rodriguez et al. [1], symmetrical multilevel inverter topologies typically involve cascaded H-bridge cells with identical voltage sources, which allow the inverter to produce a stepped output voltage waveform with low total harmonic distortion (THD). The symmetrical arrangement simplifies control and voltage balancing, making it suitable for medium- and high-voltage industrial applications [3].

According to Teodorescu et al. [2], symmetrical configurations offer reliable and efficient performance for renewable energy integration and electric drives. While the number of switching devices in SHMLI is similar to traditional multilevel inverters, the number of isolated DC voltage sources required is reduced compared to cascaded multilevel inverters, which lowers system complexity and cost without sacrificing output quality. Furthermore, advanced modulation techniques such as phase disposition PWM can be applied effectively to SHMLIs to optimize harmonic performance and minimize switching losses [5].

III. SINGLE-PHASE ASYMMETRICAL HYBRID MULTILEVEL INVERTER

Asymmetrical hybrid multilevel inverters employ unequal DC voltage sources arranged in a specific sequence to generate a higher number of output voltage levels with fewer switching devices. Peng [4] introduced generalized multilevel inverter topologies which leverage asymmetric voltage levels to increase the number of steps, thereby achieving better harmonic performance without the need for additional power devices.

The advantage of asymmetrical configurations lies in their ability to naturally reduce THD as the number of output levels increases, often eliminating the need for additional filtering [1,4]. Abu-Rub et al. [3] highlight that asymmetrical multilevel converters are promising for medium-voltage industrial applications where cost, size, and efficiency are critical factors. By carefully selecting the DC voltage source values, asymmetrical inverters can achieve better voltage utilization and performance compared to symmetrical designs with the same number of devices. This makes them especially attractive for applications where high voltage quality is essential but device count and cost need to be minimized.

IV. S INGLE - PHASE HMLI TOPOLOGY

Fig. 1 (a) and (b) exhibit the topology in a single-phase configuration. There are eight semiconductor switches in total (S1–S8). The center arm switches (S1–S4) function at a high frequency (IGBT or MOSFET), while the remaining four switches (S5–S8) form the standard H-Bridge and function at a low frequency (IGCT or GTO). The single-phase symmetrical HMLI in Figure 1(a) produces a 5-level output voltage since it has two equal-valued sources. That is, -2E, E, 0, E, and 2E. The single-phase asymmetrical HMLI (ASHMLI) in Fig.

1(b) produces a 7-level output voltage because it has two sources of unequal value -3E, -2E, E, 0, E, 2E, and 3E. [9].

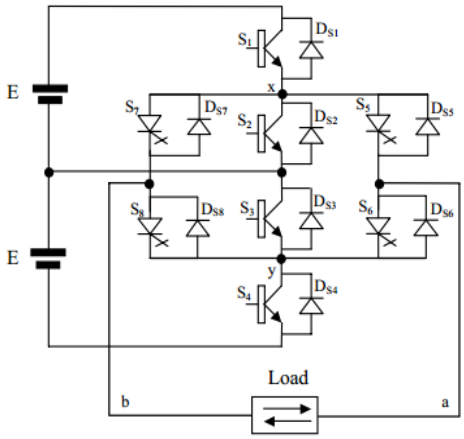

***Fig. 1(a)**: Single-phase Symmetrical HMLI*

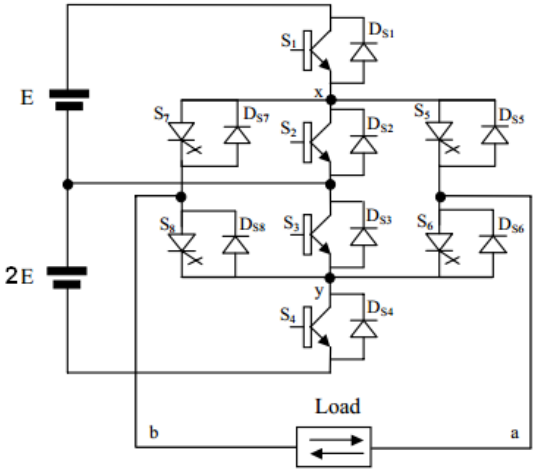

***Fig. 1(b)**: Single-phase Asymmetrical HMLI*

The control sequence for the switches to get the desired output voltage level as shown in **Fig. 2(a) and Fig. 2(b).** The switch S1-S4 produces unipolar waveform and switches S5-S8 produces alternate output voltage waveform. The modulation strategy used for triggering the switches are **(1)** phase-shifted disposition (PSD) **(2)** phase-disposition (PD) in single-phase symmetrical and asymmetrical HMLI respectively [9, 14, 6].

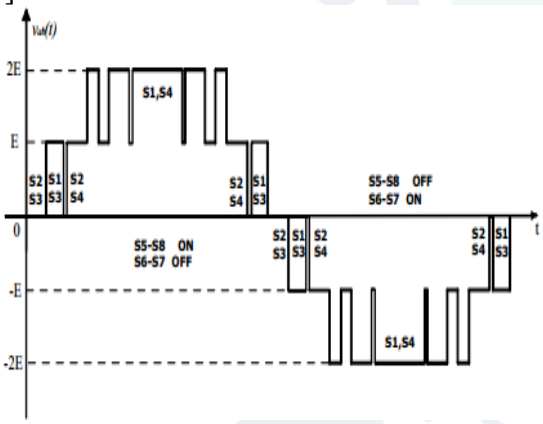

***Fig. 2(a)**: Single-phase Symmetrical HMLI*

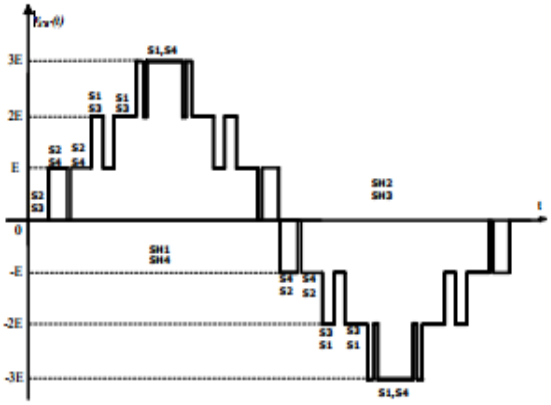

***Fig. 2(b)**: Single-phase Asymmetrical HMLI*

V. PHASE-SHIFTED DISPOSITION (PSD) MODULATION IN SHMLI

Phase-Shifted Disposition (PSD) modulation is a widely used carrier-based Pulse Width Modulation (PWM) technique applied in Single-Phase Symmetrical Hybrid Multilevel Inverters (SHMLIs) to optimize output voltage quality and reduce switching losses.[9, 14]. PSD modulation employs multiple triangular carrier signals, each phase-shifted by equal intervals, which are compared with a sinusoidal reference waveform to generate gating signals for the inverter switches.

In the SHMLI topology, PSD modulation allows the generation of multiple voltage levels by effectively controlling the timing of the switching devices. The phase shift between carrier signals distributes the switching events across the devices, thereby reducing the switching frequency per device. This leads to lower switching losses and improved efficiency, which is particularly beneficial for medium- and high-power applications [9,14].

Furthermore, PSD modulation significantly reduces the total harmonic distortion (THD) of the output voltage waveform by minimizing low-order harmonic content. The phase displacement between carriers smooths the

overall voltage waveform, providing a near-sinusoidal output without the need for bulky filtering components. This modulation technique also supports the inherent advantages of SHMLI topologies, such as a reduced number of isolated DC supplies and fewer power devices compared to traditional multilevel inverters, while maintaining excellent harmonic performance [9,14].

Phase-shifted disposition (PSD), a multicarrier PWM approach, is the basis of the modulation scheme used to drive the switches in the case of single-phase symmetrical HMLI. In this case, the modulating signal Vm is compared to two triangular carrier signals that have been moved by 180 degrees to produce the output signal. Figs. 3(a) and 3(b) depict the control circuits utilized to generate the switch command pulses using modulating and carrier signals.[9, 14].

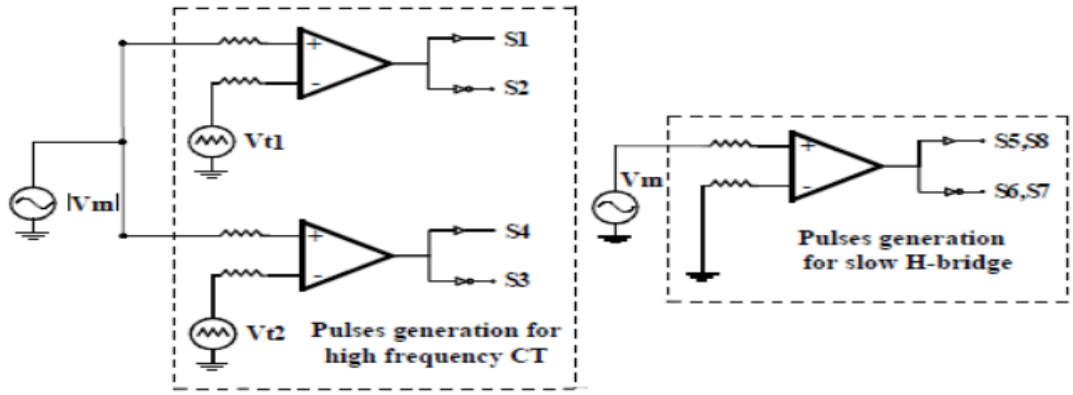

Fig. 3(a) Single-phase Symmetrical HMLI Control circuit

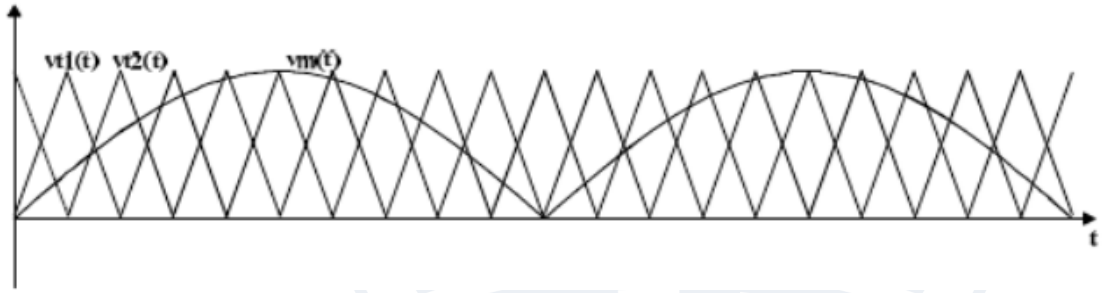

Fig. 3(b) Modulating and Carrier Control signal

VI. PHASE DISPOSITION (PD) MODULATION IN ASHMLI

Phase Disposition (PD) modulation is a common multicarrier PWM technique employed in Asymmetrical Single-Phase Hybrid Multilevel Inverters (ASHMLIs) to achieve efficient voltage synthesis and harmonic reduction. [9, 14]. PD modulation uses multiple carrier signals that are aligned in phase and stacked vertically, forming a set of triangular waveforms of equal frequency and amplitude. These carriers are compared with a sinusoidal reference waveform to generate switching signals.

In the context of ASHMLIs, which utilize unequal DC voltage sources to produce a higher number of voltage levels with fewer devices, PD modulation effectively controls the switching of power devices to produce a stepped output voltage waveform with low total harmonic distortion (THD). The alignment of carriers in phase simplifies the modulation process and improves the linearity of the output waveform, which is especially advantageous in asymmetric topologies where voltage steps vary in size [9, 14].

Moreover, PD modulation in ASHMLIs facilitates reduced switching losses and improved efficiency by controlling the switching instants carefully across different voltage levels. This modulation technique is compatible with the asymmetric nature of the inverter, ensuring that the output voltage levels are generated accurately according to the unequal DC sources while maintaining good harmonic performance [9,14].

In single-phase asymmetrical HMLI, the driving strategy of the switches produced by comparing three triangular carrier signals (all in phase but displaced vertically with a value equal to its maximum value) with a modulating signal. Control circuits used for the generation of pulses for the switches with modulating and carrier signal are shown in Fig. 4(a) and Fig. 4(b) [6].

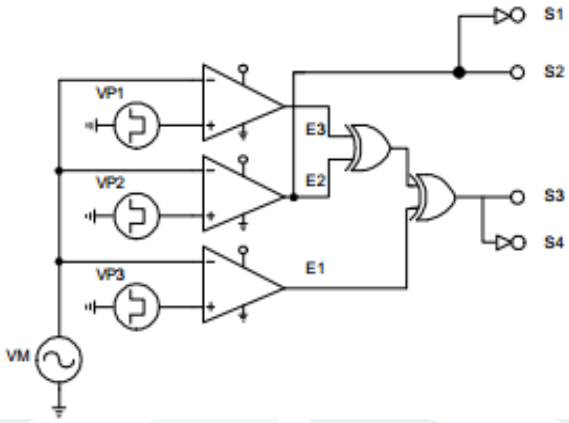

Fig. 4(a): *Single-phase Asymmetrical HMLI Control circuit*

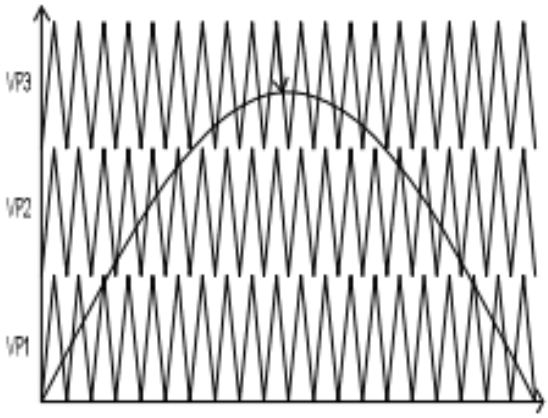

Fig. 4(b): *Modulating and Carrier signal*

VII. SIMULATION RESULTS

Eight IGBT are used in this hybrid inverter. The function of an inverter is to change a fluctuating DC to an AC. Batteries or solar cells are used to supply the cascaded circuit's input DC source. The triggering pulse applied to the switches is regulated by the use of PWM approach. We can adjust the output by varying the modulation index. Typically, the carrier wave is a triangle, while either a sine wave or a DC signal used as a reference. Compared to many semiconductor power devices, the IGBT gate triggering is crucial. The IGBT gadget features high-speed applications and quick switching capabilities. Therefore, these days, inverter circuits are where this device is mostly utilized.[8].

The simulated result after implementing above discussed modulation is as shown in Fig. 5(a) and Fig. 5(b) and their FFT analysis are also shown in Fig. 6(a) and Fig. 6(b).

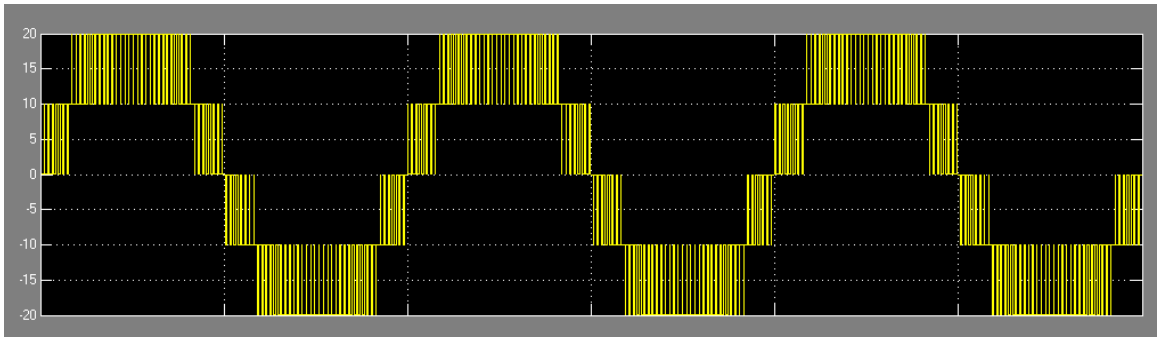

***Fig. 5(a)**: output voltage level*

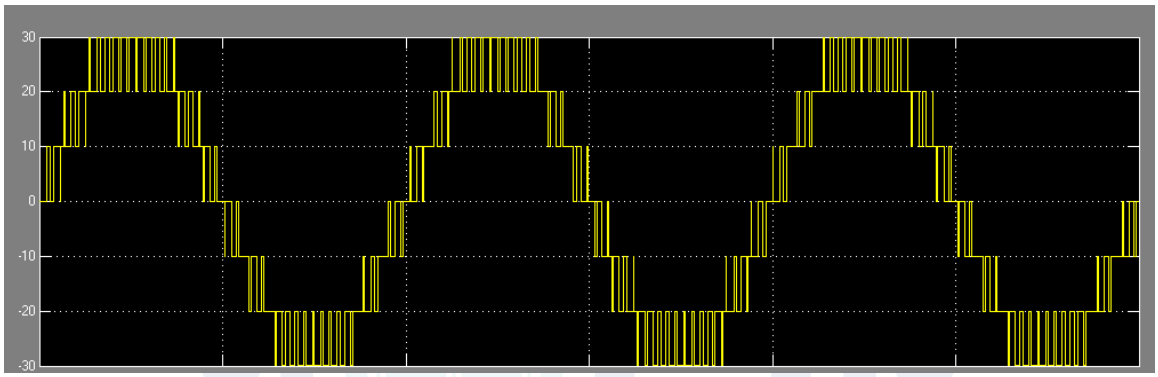

***Fig. 5(b):** output voltage level*

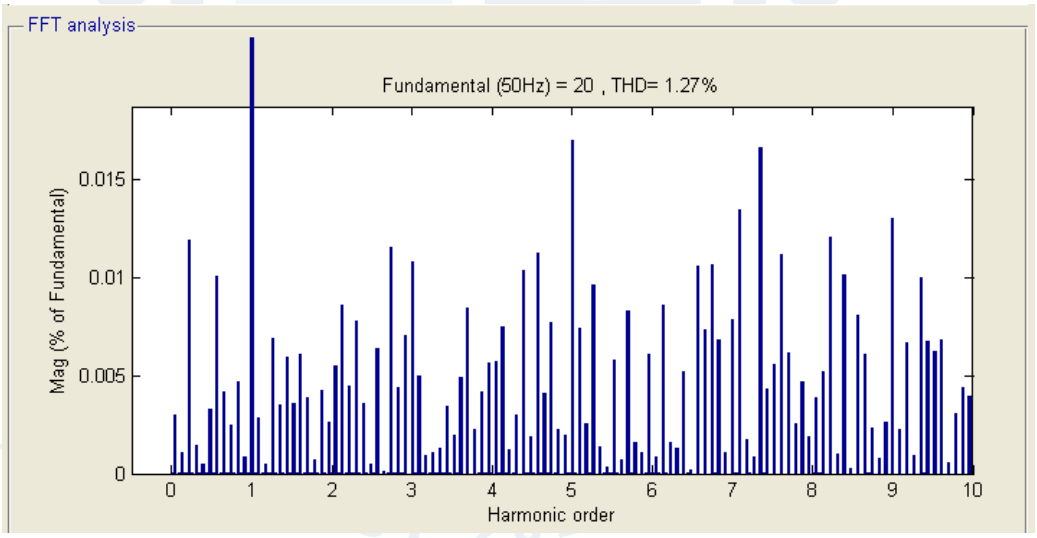

***Fig. 6(a)**: Single-phase symmetrical HMLI FFT analysis*

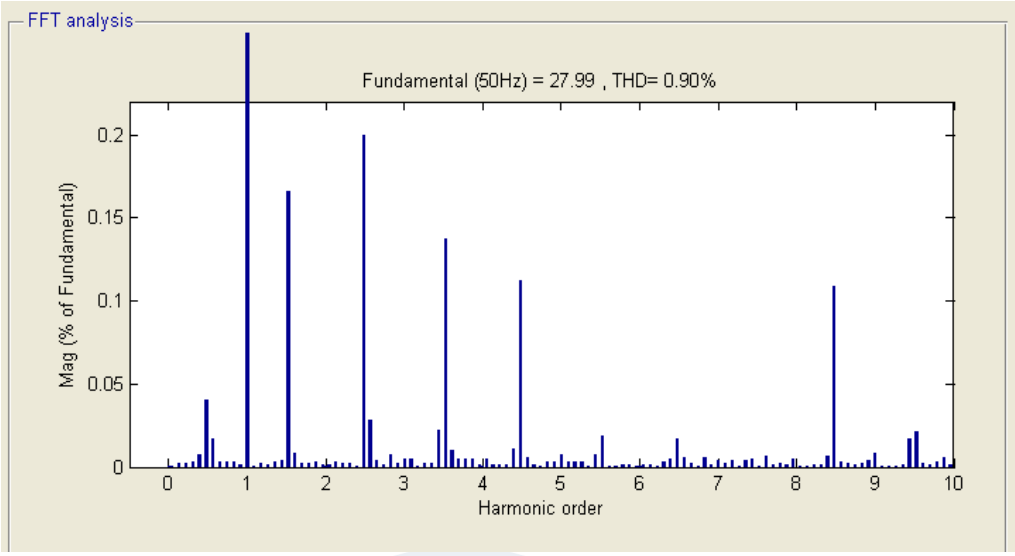

Fig. 6(b): *Single-phase Asymmetrical HMLI FFT analysis*

VIII. SIMULATION RESULLTS OF SYMMETRIC & ASYMMETRIC HMLI

INVERTEER	No. of switches	Output Voltage Level	THD (%)
SHMLI	8	5	1.27
ASHMLI	8	7	0.90

IX. CONCLUSIONS

One effective method to reduce output voltage harmonic distortion without increasing the number of power devices is the use of asymmetric multilevel converters [10,11]. The proposed circuit achieves multilevel output with low total harmonic distortion (THD) by adding only four extra switches. Asymmetric multilevel inverters can generate higher voltage levels using fewer components, and as the number of output levels increases, the THD naturally decreases to very low values, often eliminating the need for additional filtering [10].The inverter utilizes the phase disposition sinusoidal pulse width modulation (PD-SPWM) control technique. Since this approach generates only positive carriers for PWM control, it simplifies the modulation process, reducing complexity. Results clearly demonstrate that the proposed design can operate effectively as a multilevel inverter with fewer carrier signals [7]. These topologies are suitable for medium- and even high-voltage drive applications with less inductive loads. The resulting line voltage waveform meets key requirements such as low common-mode voltage and harmonic frequencies shifted away from the switching frequency. Compared to the cascaded H-bridge multilevel inverter, the Single Phase Hybrid Symmetrical Multilevel Inverter (SHMLI) reduces the number of isolated DC voltage sources required while maintaining the same number of semiconductor devices [11]. Future work can extend this analysis to include various hybrid topologies, taking into account efficiency, design parameters, and additional harmonic distortion considerations.

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